A Look at Boundary Scan From a Designer's Perspective

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Abstract

Much attention has been focused in the past on the benefits of boundary scan to the manufacturing test process and the test engineer. While ultimately the decision to use boundary scan in a given project should be based on positive impact to product life-cycle cost, the benefits that accrue to the designer are often overlooked. This paper describes such benefits to designers at all levels of product design: chip, board, system. It also provides insight into special considerations for the designer who implements or uses boundary scan.

Background

Beginning in 1985, several European and North American companies banded together to form the Joint Test Action Group (JTAG). Their stated task was to solve the problem of printed-circuit board (PCB) manufacturing test, which was growing more difficult as integrated circuits (ICs) became smaller and more complex (see Figures 1 and 2).[1,2] Their solution was eventually standardized as the IEEE Std 1149.1-1990 Test Access Port and Boundary-Scan Architecture. This standard provides for inclusion of required test resources into ICs themselves.[3]

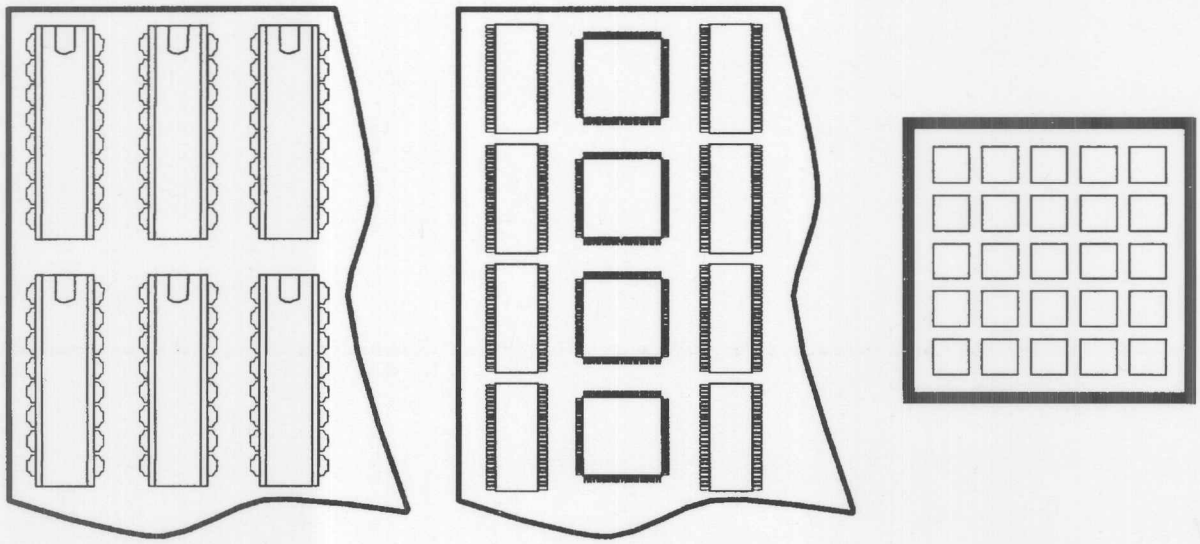

Figure 1. The Incredible Shrinking Board Results in Loss of Test Access

Manufacturing test of PCBs is essentially an effort to find defects (such as net-to-net shorts and solder opens) in the assembly of ICs and other components onto a board. This effort is obviously made more difficult by ICs that are both smaller and more complex. The ability of functional ("edge-connector") test to isolate PCB assembly defects to an adequate level is quickly thwarted by increased board functional density (see Figure 3). Since only the primary input/output are used for the test, the difficulty of test generation and the requisite test length grow dramatically as the board complexity increases.[1,2,4]

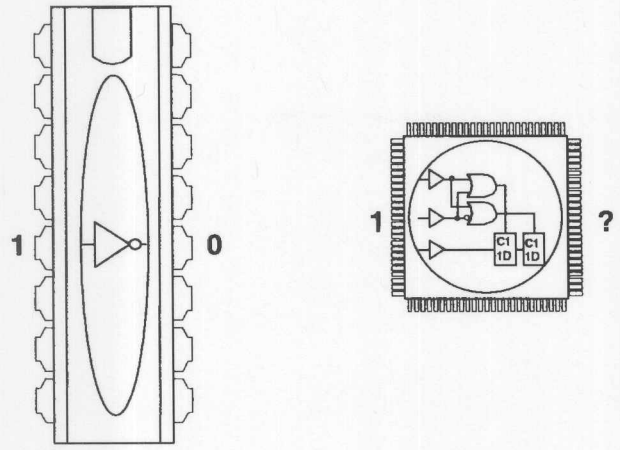

Figure 2. Increasing Integration at Chip Level Complicates Controllability

In-circuit ("bed-of-nails") test, which was an earlier attempt to improve fault isolation in complex boards, is likewise thwarted by increased IC functional density and, further, by physical constraints (see Figure 3). Since in-circuit test is based on the physical probing of (preferably all) nets internal to a PCB, smaller pin-to-pin spacing requires improvements in probe technology that are becoming increasingly more difficult and costly. In many cases, such as multichip modules (MCMs), ball-grid arrays (BGAs) and buried signal traces, physical access to internal nodes is not possible at all. Increased functional complexity of ICs causes problems because, in order to place IC outputs in known states for continuity test, the function of the device must be manipulated by often long and complex pattern sequences at IC inputs. A similar argument holds for continuity test at IC inputs.[1,2,4]

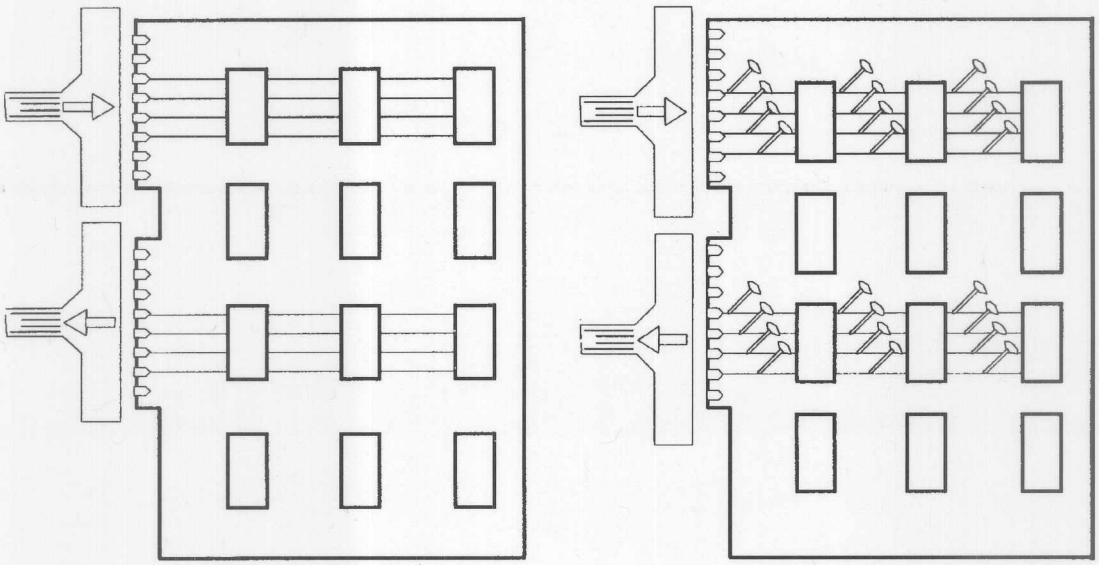

Figure 3. Traditional Methods of Board Test

The boundary-scan idea builds on the concepts of in-circuit test. However, physical probes ("nails"), which are placed mid-net, are replaced by boundary-scan cells (BSCs). These "virtual" probes are placed on-chip at IC inputs and outputs (the boundary of the IC), and are therefore placed at the net ends (see Figure 4). This results in two major improvements: (1) physical access is no longer required at boundary-scan nets, and (2) continuity test is no longer subject to IC complexity. The net effect is that the goal of manufacturing test, to isolate defects in assembly process to a pin or net, can be accomplished by highly automated test-pattern generation (ATPG).[2]

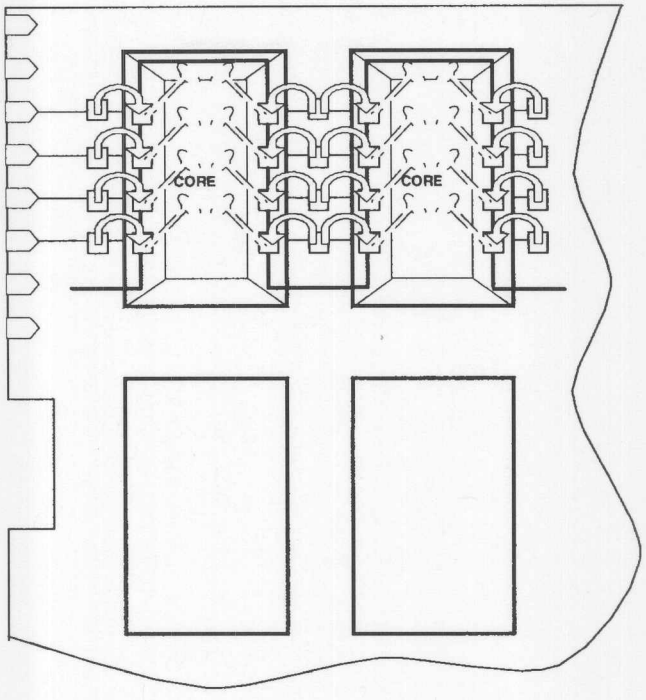

Figure 4. The Boundary-Scan Idea

Finally, in order to provide a means to arbitrarily control and observe these BSCs with minimal pin overhead, the BSCs are designed such that they can be serially concatenated to form a shift register between two IC pins, Test Data Input (TDI) and Test Data Output (TDO). The additional control structures required to select between normal and test operational modes have also been designed to minimize pin overhead and to maximize flexibility to handle test modes in addition to that used for PCB manufacturing test (see Figure 5). This Test Access Port (TAP) is based on a state machine (TAP Controller) that operates synchronously to a Test Clock (TCK, to which all operations of the test logic are synchronous) and under the control of a single Test Mode Select (TMS). The TAP Controller explicitly provides for a single instruction register that controls the test modes and for any number of test data registers (including the boundary-scan register) that can be selected by specific instructions.[2]

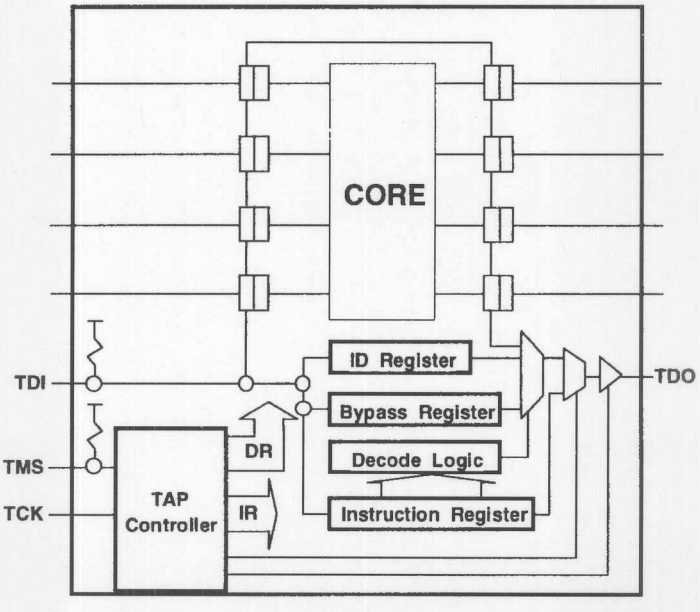

Figure 5. The Boundary-Scan Control Architecture

Standardization of the TAP and TAP Controller, as well as the boundary-scan architecture, has been key to the broad acceptance of the technology across IC, tester, and computer-automated engineering (CAE) tool vendors. Thereby, this structured design-for-test (DFT) technique may be used widely across all types of board designs by all sorts of board manufacturers, even those where catalog ICs and off-the-shelf testers and tools must be used. Additionally, the flexibility of the TAP and TAP Controller allows them to be used for access to other test features built into chip, board, or system, such as on-chip scan test or built-in self-test (BIST).[2]

Use of the Standard by the Board Designer

Since the standard has been designed primarily with board-level (test) concerns in mind, we can expect many benefits for board designers. Although many designers might deny it, they do perform at least one critical "test" operation: design verification/debug. And, just as board manufacturing test benefits from increased observability and controllability, so does board design "test" (that is, verification and debug). Boundary scan, along with other DFT techniques applied at chip or board level, can greatly aid these design test functions.

As in the case of manufacturing test, these benefits are derived in two fashions. Where boundary-scan access is provided, observability and/or controllability of a net may be obtained without concern for the function of the driving and/or receiving ICs. Also, no physical access to the board under test is required (see Figure 6). One result is that inexpensive test equipment can be used, since tester channels are needed only for the TAP and other primary I/O ("edge connector") signals. Another, perhaps more important result, is that design test can proceed even in cases where physical access to board internal nodes is difficult or impossible (due to board physical characteristics or operating environment[5]).

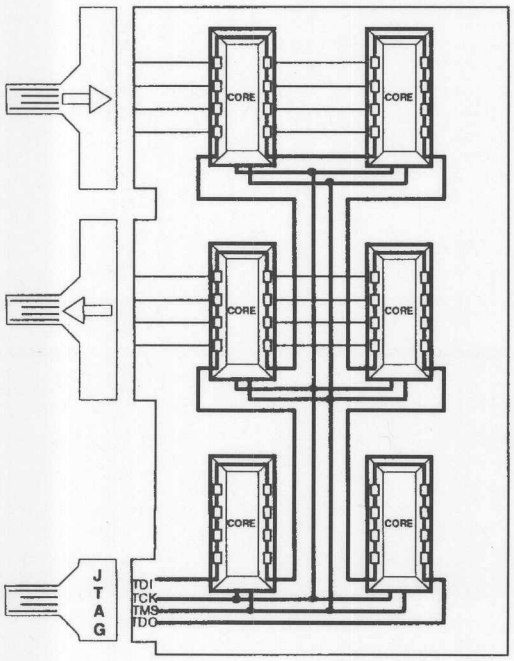

Figure 6. Board-Level Boundary-Scan Path

In the design CAE environment, the designer could have virtually any desired level of observability and controllability to board-internal and (in case of ASICs, FPGAs, or PLDs) chip-internal nodes. With the appropriate boundary-scan and chip-internal scan facilities, the designer can enjoy this same level of access to such nodes in the prototype. Further, a structural ("assembly") test of the prototype can be generated that can be applied from this inexpensive test equipment and without need for expensive test fixturing. Such a test can be automatically generated, given the board netlist and descriptions (in the boundary-scan description language, BSDL) of the boundary-scannable devices. This simple test is available even when manufacturing test program, equipment, and fixtures are not (as is most often the case for prototypes, since they are difficult to provide for an unproved design). Such a test can save many frustrating hours (a testimonial indicates a reduction from 6 weeks to only 2 days[6]) which would normally be required to separate assembly problems from design problems. This is especially important if new and unproved assembly processes have been developed for the board.[5,7,8,9,15]

In some cases, the provision of boundary scan and DFT can permit some prototype testing to begin even in the absence of "key" components. For example, if a processor board were designed with proper planning, associated memory could be tested by emulating the processor, or vice versa.[10]

In addition, the actual design time and manufacturing cost of PCBs may be reduced by elimination of test points.[7,11] If enough test points can be eliminated (one example cites a reduction from 40 down to 4[6]), then possibly some PCB layers can be eliminated as well, which might greatly decrease PCB cost. In some cases, such elimination of test points may be critical to the very miniaturization goal that drives the choice of extremely dense packaging options such as BGAs.[6]

The board designer can obtain these benefits by specifying the use of boundary scan in proprietary ASICs and by placing boundary-scannable catalog (including user-programmable) components wherever possible. The task of finding such components is becoming less difficult daily as the number of such products grows. As of this writing, it has been reported that boundary scan is supported by 22 ASIC vendors, 24 vendors of over 120 standard components and 12 vendors of user-programmable logic (see Figure 7).[12]

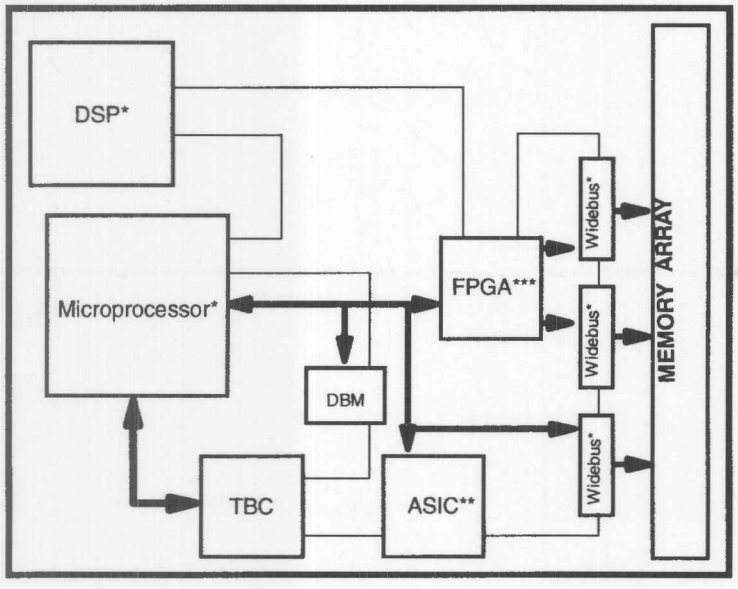

Figure 7. IEEE 1149.1 in Action

Included in such offerings are boundary-scannable bus-interface devices. These reasonably inexpensive components can replace their nonscan counterparts to gain all the above benefits. It may be useful in some cases to insert such devices even where they are not required for normal system function (for example, in parallel to a bus that is not boundary-scannable for performance reasons) in order to improve test access.[13] Often such components may bound simple clusters of nonscannable logic that can be tested using the "virtual nails" of these devices for simple "virtual" in-circuit testing (see Figure 8). Additionally, some vendors offer built-in parallel-output pattern generators and parallel-input signature registers that allow the board designer to implement board-level BIST capabilities that provide high fault coverage with very little test pattern generation.[7,14]

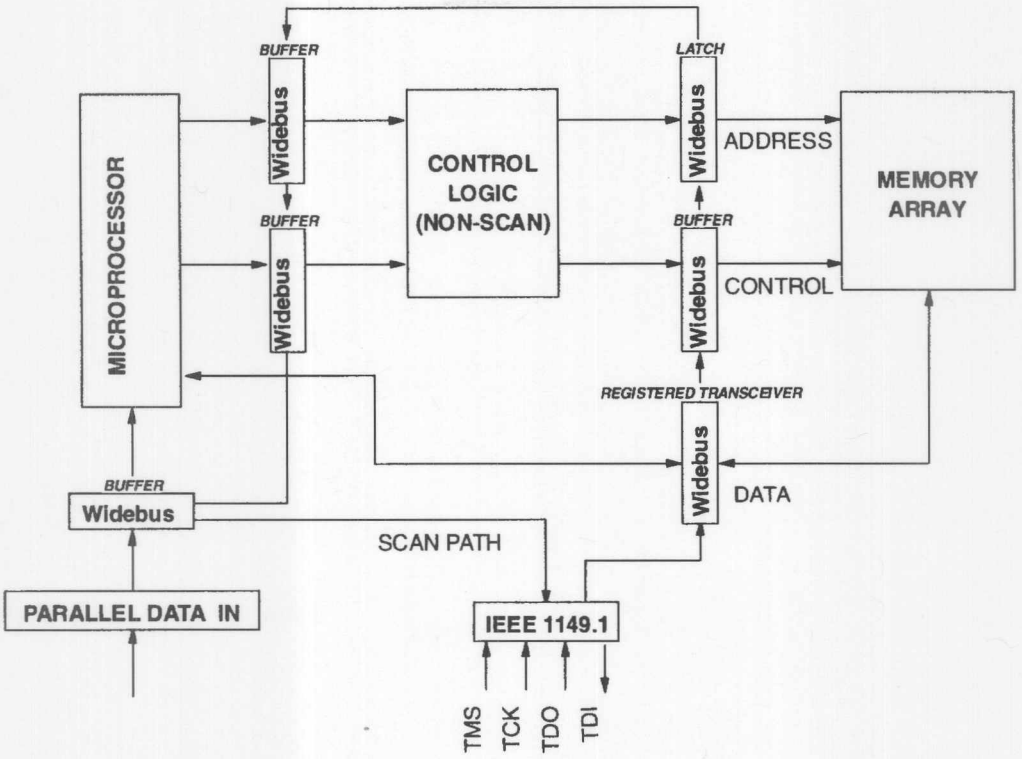

Figure 8. Logic Cluster Test

In designing the board-level scan chain, a single, simple scan chain is recommended.[4,15] Simple buffering of the TCK and TMS signals should be used, and care should be exercised in the routing, termination, and timing of these signals.[4,10,14] In the prototype, all TAP signals should be checked for signal integrity at their destinations.[10] Failure to maintain signal integrity at these signals may cause improper movement of the TAP controller and premature or unintended entry of device(s) into test modes, such as EXTEST. In such modes, the outputs of the device(s), which would be controlled from the boundary-scan register, might come into contention with those of other scannable or nonscannable devices. In general, the board designer must beware of conditions in which scannable and nonscannable drivers might be in conflict.[4]

Another key to obtaining such benefits will be access to enabling CAE tools. As of this writing, it has been reported that 14 CAE vendors supply tools that support boundary-scan test.[12] These tools fall roughly into three classes: boundary-scan insertion, access analysis, and boundary-scan ATPG. The topic of boundary-scan insertion, since it is a chip design activity, will be discussed later.

Access analysis tools examine board designs prior to layout for nets to which physical test access is not required. Such tools will identify nets in at least three categories: pure boundary-scan (all connected devices have boundary scan), mixed boundary-scan (some, but not all connected devices have boundary scan), and nonboundary-scan (no connected devices have boundary scan).[16] These nets will then be prioritized (in the stated order) for test-point elimination. Such information is then passed to a layout tool (or designer) for elimination of the test points, as required for optimal board layout and fabrication cost.[17]

Boundary-scan ATPG tools automatically generate prototype or manufacturing tests to be applied to the board under test using the board-level TAP. Some of these tools can consider physical access (via in-circuit "bed-of-nails") as well. The best-in-class tools of this type will generate tests for TAP and BSDL validation, and board-level scan-path integrity. These tests, in combination, verify the infrastructure for applying remaining tests. The best-in-class tools generate the following additional types of test for board structural test: boundary in-circuit, virtual interconnect and interactions, and virtual cluster/component test. Boundary in-circuit test uses physical access, but utilizes boundary-scan for simple access to on-chip inputs and outputs for reduced test generation time and complexity. Virtual interconnect and virtual cluster/component tests allow for removal of some or all physical access for test of interconnect and of nonscannable logic clusters, respectively. Such tests will include diagnostics of board assembly faults to the pin. Some tools support multiple board-level scan chains, while others support only a single chain.[6,12,16,17,18]

Some means of boundary-scan test application is required. In some cases, this may be in-circuit or board-functional test equipment that is already owned, perhaps with some modifications to handle deep serial patterns. In other cases, it may be an inexpensive test adapter for PC or workstation. Such "testers" must, at a minimum, exercise the board-level TAP(s) under control of a simple vector file. In either case, to get the most out of boundary scan in design debug, an interactive scan-based diagnostic capability is desired.[10]

The best scan-based diagnostic tools will use a scan-path management database that permits interactive view and control of only those portions of the board (pin, register, bus, or user-defined signal group) that are of interest (see Figure 9). Such tools completely hide the complexity of the TAP protocol and boundary-scan chain from the user and allow efficient design debug in the fashion of parallel stimulus generators and logic analyzers to which the design engineer is accustomed. In fact, the best such tools include logic-analyzer-like waveform and state table displays.[19]

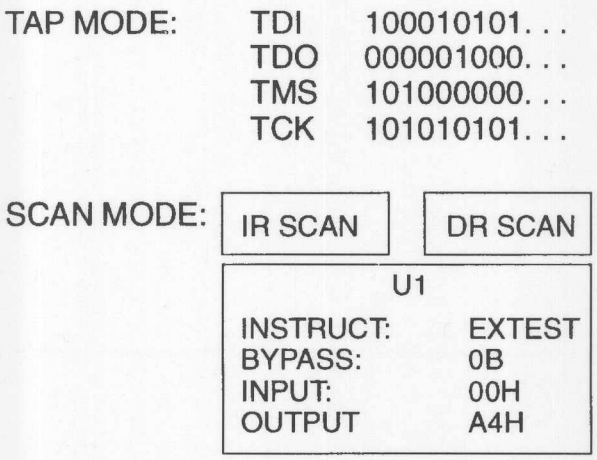

Figure 9. Scan-Path Management

Such tools should also support multiple test vector generation methods: interactive, CAE parallel (with automated serialization), and boundary-scan ATPG (based on a standard interchange format such as the Serial Vector Format, SVF). They should also describe the boundary-scan hierarchy using industry standard formats such as BSDL, the Hierarchical Scan Description Language (HSDL), and EDIF (Electronic Design Interchange Format) netlist. And, they must be sensitive to board-level constraints so that physical damage to the board, which might result from improper control of boundary-scan drivers, does not occur.[19]

Finally, they must support scan test and test reuse across all product phases. This means they must allow access to chip-internal scan and BIST, as well as board-level BIST capabilities. They must provide a flow of test information from chip to board to system. Ideally, they will provide a flow to embedded system test, enabling system built-in test based on reuse of scan-based test.[10,19]

Use of the Standard at Chip Level

At chip level, the standard provides most benefit in its provision for a standard test access method (the TAP) which allows access to chip-internal test facilities in addition to the required boundary-scan test facilities. Such chip-internal test facilities include internal scan path, BIST, and built-in emulation and debug.[5,7,8,10,17,20]

Chip-internal scan path involves the substitution of normal storage elements (latches and flip-flops) with scannable counterparts that can be serially interconnected for test purposes. In a full-scan approach, all such storage elements are replaced, and the circuit is thereby partitioned into blocks of combinational logic between parallel inputs and outputs of a simple shift register. Robust combinational ATPG algorithms can then be used for rigorous structural test of the chip logic. Partial scan implies the replacement of only selected storage elements. It is used in cases where chip area and performance cannot be traded-off for improved fault coverage. However, since not all storage elements are scanned, some sequential ATPG must be used. The failing of such ATPG to provide adequate fault coverage is the primary reason for adopting chip-internal scan in the first place.[21]

BIST uses on-chip stimulus generators and response monitors to eliminate the need for any test generation. Most commonly it uses pseudo-random pattern generation and signature analysis (cyclic redundancy checking) implemented in linear-feedback shift-registers (LFSRs). In such cases, care must be taken that the circuit to be tested is not resistant to pseudo-random techniques. Where the circuit is not suitable for pseudo-random techniques, deterministic BIST methods are possible.[22]

Such features are often most powerful when used in combination. For instance, if boundary-scan and chip-internal scan path are both implemented so that they may be used simultaneously in a given IC, then static test application requirements can be reduced to only the four TAP signals, since the boundary-scan register can control/observe the primary inputs/outputs to the core logic (see Figure 10).[22] If internal scan path is combined with BIST, the BIST may be used for quick pass/fail testing while the internal scan is used for chip debug and failure diagnosis. Additionally, if a standard RUNBIST capability is provided, the end user may perform quick function testing while the IC is in-system.[23]

Finally, boundary scan alone can reduce test access requirements to the TAP only. The same static functional vectors that would be applied by an expensive IC tester with many parallel channels can be applied through boundary scan (if INTEST capability is provided). Setup of ICs for parametric test can also be facilitated by boundary scan. And boundary scan can be used in hostile environments where physical access is difficult or impossible.[5] For mixed-signal ICs, inclusion of boundary scan can provide a very useful partitioning of analog and digital functions, allowing each to be tested independently (see Figure 10).[24]

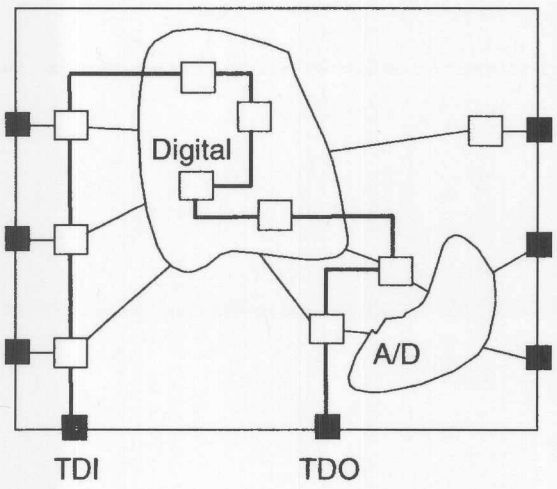

Figure 10. Boundary Scan Plus Internal Scan in Mixed-Signal Circuit

To benefit from these capabilities, they must be designed into the chip. Several types of CAE tools can aid this process. Most such tools provide for some level of automation of internal (full or partial) scan, BIST, and boundary scan. The abstraction level at which these tools operate ranges from register-transfer level down to gate level, and the point of use ranges from pre-synthesis to post-synthesis (or schematic capture). In the area of internal scan insertion, the best tools will provide full scan insertion and partial scan insertion driven from chip area, performance, and test coverage constraints. They will also provide the combinational and/or sequential ATPG needed to capitalize on the scan path.[6,12,21]

Boundary-scan insertion tools are similarly varied. Capabilities to look for besides automated insertion of TAP and boundary-register are BSDL output, test pattern generation for standard-conformance checking and BSDL validation. Some tools use BSDL (or graphical entry) as an input, rather than an output, to the boundary-scan insertion process.[18]

The need for validation of BSDL and TAP integrity cannot be overstated since the entire test infrastructure is based upon proper operation of these components.[4,17] Special attention should be given to TAP pin placement and to considerations for proper clocking of internal scan path relative to boundary-scan path.[4,25]

Use of the Standard at System Level

Finally, the standard can bring benefits to design at system level also. Such benefits are primarily derived from the ability for TAP-accessed tests to be reused at higher levels of product integration, from chip to board to system.[1,7] These capabilities may be used for system hardware debug and hardware/software integration while chips and boards are in their normal system configuration and operating environment. Since no physical access is required, use of "extender" cards, complex connectors, and large environmental control systems is not needed.[5,7,8]

Additionally, boundary scan and other TAP-accessed test facilities may be useful in meeting system design requirements for built-in test, field service test, and remote diagnostics. Clearly, in most such cases it is desirable to limit the expense and complexity of test equipment required. Boundary scan can facilitate this by limiting test access and control requirements to an inexpensive diagnostics port (the TAP).[7,20]

Boundary-scannable bus-interface devices can be useful in these applications, as well, by partitioning the system along field-replaceable unit (PCB) boundaries. Also, if the backplane interface of PCBs is scannable, then backplane connectivity and integrity testing can be performed. By using the previously mentioned pattern generation and signature analysis techniques, it is even possible to perform gross performance testing on the backplane.[14]

One problem in the area of system implementation of TAP access is referred to as the multidrop problem (see Figure 11). Since TDI and TDO are serial terminals, they must be daisy-chained in simple chains. This "ring" configuration presents a problem in backplane-oriented systems, since some boards may be removed, disabling the scan chain. An alternative, proposed by the standard, is the "star" configuration which allows TDI and TDO pins on PCBs to be bussed.[3] However, since multiple TMS signals are required to prevent simultaneous scanning (and thereby contention on TDO bus) of PCBs, many backplane routing channels are required. Several alternative multidrop schemes, based on serial addressing techniques, have been proposed to alleviate this problem. The best of these techniques will enable multidrop routing of backplane signals, with minimal need for test reformatting and minimal impact on test application time.[1,4,6,7,20,26]

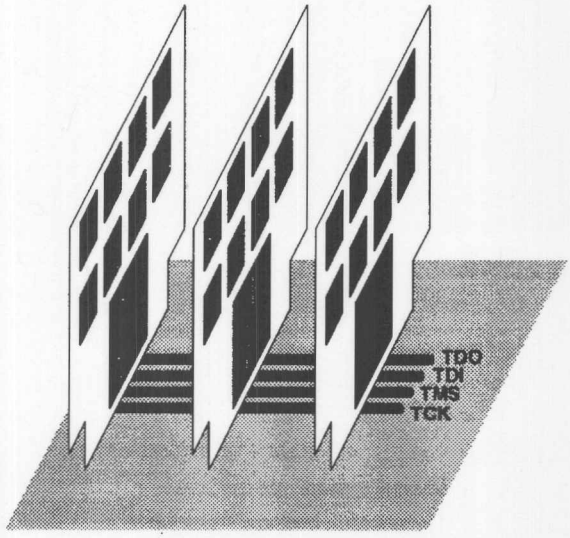

Figure 11. Multidrop System TAP

Conclusion

We have discussed many benefits that are available to designers through use of the Test Access Port and Boundary-Scan Architecture. These benefits are primarily in the area of design verification and debug and are enabled by improved controllability and observability into circuits, and freedom from physical access constraints provided by boundary scan. While some effort is certainly required to derive such benefits, a suite of CAE tools that reduces such effort has been presented. Designers at all levels of product integration (chip, board, system) are encouraged to evaluate boundary scan for benefits that they and their companies may derive from its use.

Acknowledgement

The author of this document is Adam W. Ley.

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Design Tradeoffs When Implementing IEEE 1149.1

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Introduction

This paper explores the many design tradeoffs that occur when implementing the IEEE 1149.1 test bus in integrated circuits (IC), printed wiring boards (PWB), and systems. As with any design task, tradeoffs must be made to achieve the best mix of functionality, testability, reliability, producibility, and maintainability. As an industry-wide standard, the IEEE 1149.1 test bus and boundary-scan architecture allows a consistent method for circuit controllability and observability across all levels of development and test. Test and debug operations can be performed via the IEEE 1149.1 test bus and boundary-scan architecture in many areas including design verification, fault troubleshooting, factory board and system test, and field test without requiring actual physical access. Embedded test features, which previously could be accessed only at one test level, can be accessed easily at each level of integration (i.e., IC, board, subsystem, and system).

Test Considerations – Ad Hoc/Structured

There are two fundamental ways to apply testability to a design: ad hoc (or unstructured) and structured. Ad hoc testability is simply intended to solve a particular test problem (i.e., adding a test point to observe a signal line during board test). While this may be useful for a particular test environment, in this case factory board test, it may not be useful for any other test environment, such as IC or system test. Structured testability, on the other hand, is designed to be useful at several levels of test. For instance, an IC with built-in self test (BIST) and a standard test interface can be used for IC test, board test, and system test. This type of testability is considered structured because it is standardized and can be used in several test environments.

What is IEEE 1149.1?

The IEEE 1149.1 test bus and boundary-scan architecture allow an IC, and similarly a board or system, to be controlled via a standard four-wire interface. Each IEEE 1149.1-compliant IC incorporates a feature known as boundary scan that allows each functional pin of the IC to be controlled and observed via the four-wire interface. Test, debug, or initialization patterns can be loaded serially into the appropriate IC(s) via the IEEE 1149.1 test bus. This allows IC, board, or system functions to be observed or controlled without actual physical access.

The IEEE 1149.1 test bus comprises two main elements: a test access port (TAP), which interfaces internal IC logic with the external world via a four-wire (optionally, five-wire) bus; and a boundary-scan architecture, which defines standard boundary cells to drive and receive data at the IC pins. IEEE 1149.1 also defines both mandatory and optional opcodes and test features. The test bus signals are: Test Clock (TCK), Test Mode Select (TMS), Test Data In (TDI), Test Data Out (TDO), and the optional Test Logic Reset (TRST). The IEEE 1149.1 specification also specifies that the ICs can be connected in either a ring or star configuration. A simplified block diagram of the architecture is shown in Figure 1.

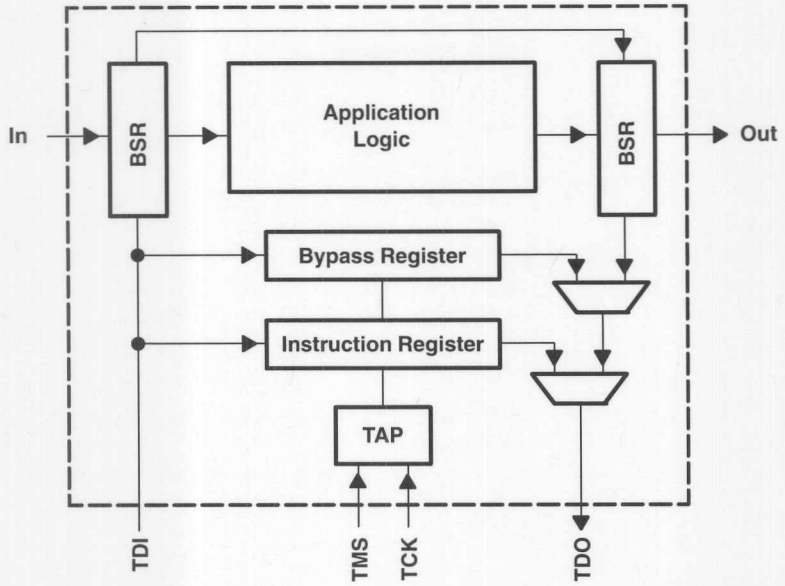


Figure 1. IEEE 1149.1 Scan-Bus and Boundary-Scan Architecture

Overview

Design Costs Versus Test Costs

Cost is a driving requirement when designing any system. Design costs are easily calculated in terms of part costs, manufacturing assembly, engineering design labor, etc. Test costs are also quantifiable but may not be done as easily. Certainly, test equipment and test software development costs can be readily calculated, but test times, troubleshooting, and repair are not as obvious. In complex designs or designs that have long service lives, the life-cycle costs (LCC) of the product are dominated by test and maintenance costs, not design and production costs. It is typical to "invest" time and money to design for test, which then saves production and maintenance costs. To provide an easy and cost-effective method to include IEEE 1149.1 testability into any design, Texas Instruments (TI) has developed a family of testable ICs and Application-Specific Integrated Circuit (ASIC) cells, These ICs and ASIC cells are members of the System Controllability, Observability, and Partitioning Environment (SCOPE™) family.

Use of Scannable Parts

Two complementary techniques are used when designing IEEE 1149.1 into a system: off-the-shelf parts (i.e., TI SCOPE bus-interface products) and ASICs. Each satisfies a particular application, but both can be used together in the same design. TI SCOPE bus-interface products and other off-the-shelf parts are suitable when testability is needed in a functionally equivalent device. Consider a simple PWB with a processor and memory. Without testable SCOPE bus-interface products, the address and data buses would have to be tested indirectly by writing and reading memory via the processor. The embedded address and data buses buffered by '244 and '245 parts can be replaced by functionally-equivalent IEEE 1149.1-compliant TI SCOPE bus-interface products. Now, tests of the address and data buses can be achieved by controlling and observing the SCOPE bus-interface products via the IEEE 1149.1 test bus. Addresses and data can be explicitly loaded and driven by the SCOPE bus-interface products or functionally-driven addresses and data can be captured and read via the IEEE 1149.1 test bus.

The other technique used to incorporate IEEE 1149.1 features into a design is by designing it into ASICs. If ASICs are used, adding IEEE 1149.1 is a straightforward and efficient method of implementing testability into a design.

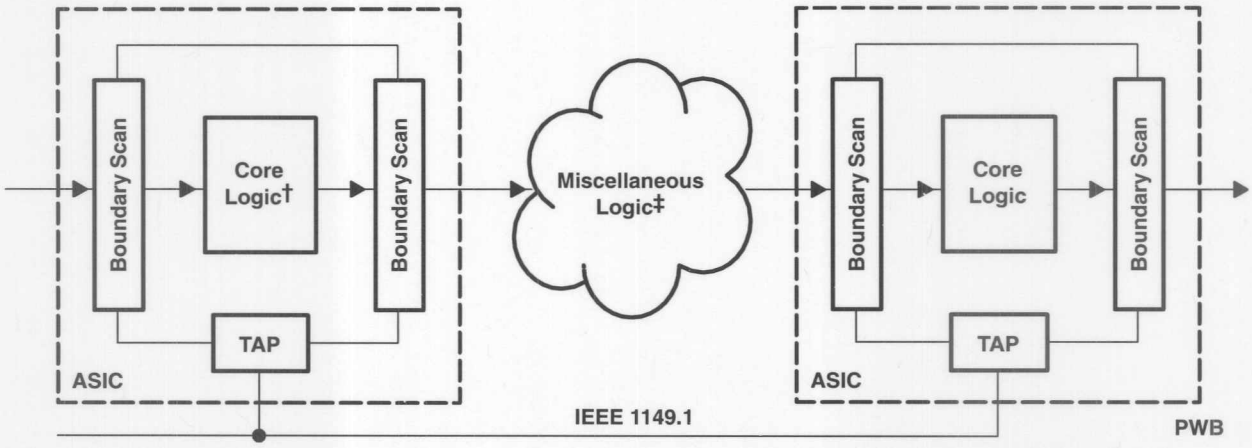
TI also produces several other IEEE 1149.1-compliant test ICs to support PWB and system test. A test-bus controller (TBC) is available to drive the IEEE 1149.1 test bus. Other members of the SCOPE family include scan-path selectors (SPS) to partition long scan paths into multiple small chains and a digital bus monitor (DBM) to monitor and capture data in real time.

Design Tradeoffs in Implementing IEEE 1149.1 IC Level

The following paragraphs present IEEE 1149.1 design tradeoff information at the IC level. While this data is useful in simply comparing IEEE 1149.1 ICs to non-IEEE 1149.1 ICs, this one-to-one comparison is not as useful as comparing the total advantages/disadvantages at the PWB and system levels. Total PWB and system-level tradeoffs, not IC tradeoffs, should be used to determine the final implementation strategy.

Controllability and Observability

Obviously, in addition to performing their functional tasks, the SCOPE family of test products provides a level of controllability and observability that was previously unachievable. During design verification, test, or troubleshooting, signal states may be sampled or controlled via the IEEE 1149.1 interface. Testing can be accomplished on the internal IC logic via pins-in testing, or tests on external IC logic or interconnects via pins-out testing. Pins-in testing is accomplished by loading IC input pins via the IEEE 1149.1 interface, driving the internal logic of the IC, capturing the output pin states, and scanning out the results. Pins-in testing is accomplished by loading IC output pins via the IEEE 1149.1 interface, driving the IC outputs and interconnects, capturing the data at the next IEEE 1149.1 ICs input pins, and scanning out the results. Pins-in and pins-out testing is shown in Figure 2.



† Pins-in testing is accomplished by loading test patterns at IC inputs, driving data across IC logic, and capturing patterns at IC outputs.
‡ Pins-out testing is accomplished by loading/driving test patterns at IC outputs and capturing patterns at the next IC's inputs.

Figure 2. IEEE 1149.1 Pins-In and Pins-Out Testing Via Boundary Scan

BIST/Additional Hooks

In addition to the standard four-wire interface and boundary-scan architecture that IEEE 1149.1 defines, other test or debug "hooks" can be implemented and controlled. For ASICs, it is very common to include some form of BIST to assist in device testing. IEEE 1149.1 provides a standard interface to initiate BIST and retrieve results. Two common BIST methods known as pseudorandom pattern generation (PRPG) and parallel signature analysis (PSA) are supported in the SCOPE bus-interface products and ASIC standard cell libraries. PRPG provides the capability to generate pseudorandom patterns to stimulate a circuit under test. PSA allows a stream of patterns to be collected and compressed into a unique signature. In addition to boundary scan, ASICs and other special-purpose ICs may incorporate internal scan within the IEEE 1149.1 architecture. Internal scan may be used to partition the IC into more easily testable functions, write/read internal registers, etc. TI's later generations of digital signal processors (DSPs) incorporate internal scan to provide built-in in-circuit-emulation features for test and debug. Via the IEEE 1149.1 interface, registers can be loaded/examined and the processor execution can be controlled to RUN/STOP, SINGLE-STEP, etc.

IC Pins/Package Size

The first requirement when implementing IEEE 1149.1 is the addition of four extra pins. This overhead is always required, but is less obvious in larger package devices. Table 1 shows the percent of additional pins per package size.

Table 1. 1149.1 IC Package/Pin Ratio

IC PACKAGE SIZE (NO. OF PINS)	IEEE 1149.1 IC PINS VS TOTAL IC PINS (%)
24	16.7
40	10
64	6.3
100	4
132	3
160	2.5
208	1.9

Gate Count

The number of gates to implement IEEE 1149.1 is driven primarily by the number of IC I/O pins. The reason is that IEEE 1149.1 requires each functional I/O pin to have a boundary cell. Naturally, low-gate-count ICs with a high number of I/O pins will have proportionally more gates to implement IEEE 1149.1. Some typical gate counts from a 1.0-μm standard-cell and gate-array library are shown in Table 2.

Table 2. ASIC SCOPE Cell Gate Count

IEEE 1149.1 FUNCTION	NUMBER OF GATES
Test access port (TAP)	≈183
Instruction register	≈20 gates/bit
Bypass register	≈8 gates
Unidirectional SCOPE boundary cell (hard macro) (standard cell)	≈15 gates/pin
Bidirectional SCOPE boundary cell (standard cell)	≈19 gates/pin
Unidirectional SCOPE boundary cell (soft macro) (standard cell)	≈24 gates/pin

The formula below can be used to estimate the IEEE 1149.1 gate count overhead. (Remember to count only the number of functional I/O pins, not power, ground, or unused pins).

$$\text{Total IEEE 1149.1 gate count} = \text{TAP} + (\text{IR} \times \text{IR bit width}) + \text{BR} + (\text{no. I/O pins} \times \text{no. gates/pin}) \quad (1)$$

Figures 3 and 4 show the relationship between functional gate count versus IEEE 1149.1 test logic versus pin-count increase for both standard-cell and gate-array designs.

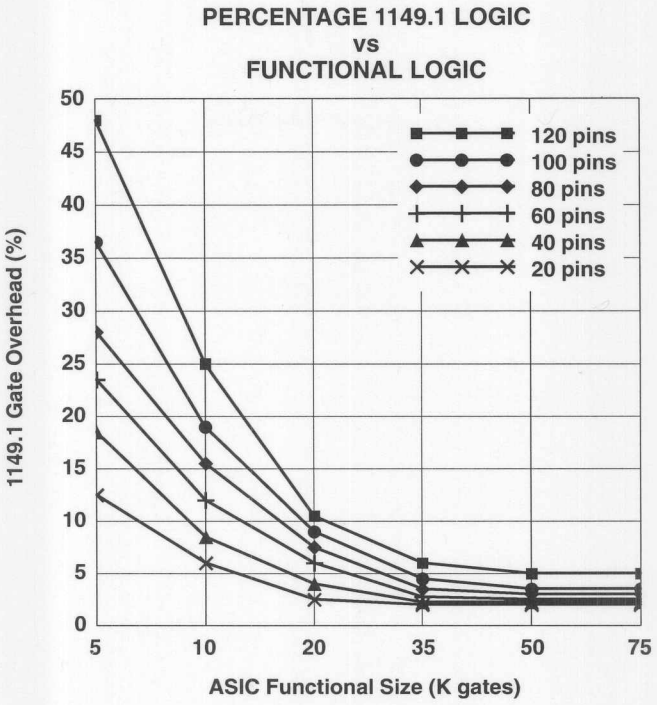


Figure 3. Standard-Cell ASIC 1149.1 Overhead

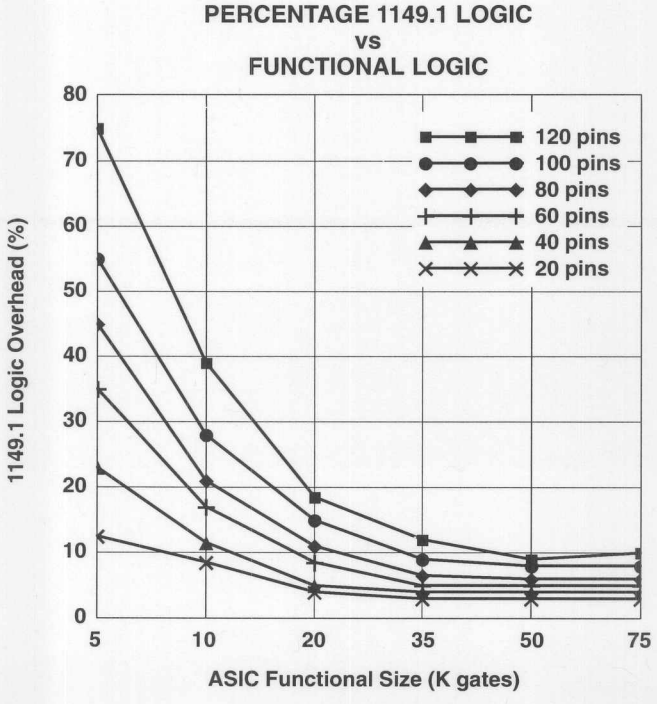


Figure 4. Gate-Array ASIC 1149.1 Overhead

Some actual ASIC examples are shown in Table 3. The first small ASIC was implemented in a gate array. The gate-array boundary cells were constructed as soft macros and therefore required more gates per pin to implement than the SCOPE hard macros. Although the IEEE 1149.1 overhead of the first ASIC may seem excessive, this ASIC acted as a translator and buffer between a processor and memory bus. The IEEE 1149.1 boundary scan provided partitioning and allowed independent testing of the functions via IEEE 1149.1. Since the first ASIC was implemented in a 6K gate array, the gates to implement IEEE 1149.1 were essentially free (they were already on the silicon). The second and third ASICs were implemented as standard-cell hard macros. Also notice that they implement BIST functions to autonomously test functions within the ASICs.

Table 3. Overhead Examples of Implementing IEEE 1149.1 and BIST

ASIC SIZE	IC FUNCTION	1149.1†	BIST	TEST TOTAL	TEST AS % OF TOTAL
4,753 gates‡	2,263	2,490	0	2,490	52.4
20,000 gates§¶	18,350¶	1,650¶	1,000¶	2,650	13.3
87,000 gates§	84,262	1,634	1,104	2,738	3.1

† All ASICs have 70 I/O pins.
‡ Implemented in gate array
§ Implemented in standard cell
¶ Gate count estimated.

Propagation Delay

The controllability and observability achievable with IEEE 1149.1 is accomplished by adding a 2-to-1 multiplexer in the normal data path. This simple solution minimizes propagation delays, yet still allows signal lines to be sampled or driven. The propagation delay of the 2-to-1 multiplexer is dependent on the technology used to implement the device. The propagation delays for a 1.0-µm CMOS ASIC library are approximately 1.0 ns (typical) for a standard-cell hard macro and approximately 1.8 ns (typical) for a gate-array soft macro. Propagation delays will naturally continue to decrease as technology matures.

Reliability

Increased gate count will slightly reduce IC reliability. However, the only functional reliability impact will come from the 2-to-1 multiplexer in the functional data path. This 2-to-1 multiplexer accounts only for two gates per boundary cell. For example, in an 8,000-gate ASIC with 100 functional pins, the 2-to-1 multiplexer only amounts to a 2.5% gate-count increase in the functional data path. This is a very small reliability impact.

Power

Power dissipation is driven by the technology used and the amount of additional IEEE 1149.1 logic. For CMOS technologies, power dissipation increases with clock frequency and gate count. Since most of the test logic (except the 2-to-1 multiplexer in the functional path) remains in a static state, the power consumption of the test logic is small.

Test Costs

The costs of IC test for IC production test and incoming inspection varies greatly with the complexity of the IC. For simple ICs, such as the SCOPE bus-interface products, there is only a slight advantage in using IEEE 1149.1 in an IC-level test. For medium- to high-complexity ICs, such as ASICs and VLSI devices, an IC test using IEEE 1149.1 provides several benefits. First, ASIC and VLSI devices can be tested statically or at low frequencies using the IEEE 1149.1 pins-in and pins-out test methods. Actually, an IEEE 1149.1-based pins-in tester has been demonstrated that simply consists of an IC socket with power, ground, and an IEEE 1149.1 TBC. Test patterns are loaded and captured inside the IC via the IEEE 1149.1 test bus. This method provides a quick, inexpensive method to verify basic IC functionality.

IC test-development costs can be greatly reduced by using the same test patterns used for IC design verification, simulation, and IC tests. The simulation patterns, or a subset, are applied via the IEEE 1149.1 test bus as previously described. The second major benefit of the IEEE 1149.1 test bus is the ability to control and examine internal nodes or states of ASIC and VLSI devices. Hard-to-test functions can be partitioned via internal scan and tested independently with smaller, easier-to-test partitions. An ASIC that may require 2^{20} (1 million) test patterns just to test a 20-bit counter can be tested in a fraction of the patterns by implementing internal scan on the counter. Patterns can be downloaded directly via scan to test any count sequence. A recently developed ASIC with very long counter chains saved over four-million test patterns by implementing internal partitioning controlled via the IEEE 1149.1 test bus.

IC Costs

IC purchase costs with IEEE 1149.1 are higher than their equivalent untestable versions. The cost delta varies, depending on the proportion of IC pins and test logic to functional pins and logic. For larger ASICs, the cost increase is small, but even in small ASIC designs the PWB and system test benefits are realizable. For I/O-limited ASICs (ASICs that have unused core gates), the cost increase is typically less than the proportional gate increase. For core-limited ASICs (ASICs that do not have spare gates), the cost may be proportional to the increase in gates, or possibly higher.

PWB Design

The following paragraphs review PWB-level advantages/disadvantages when implementing designs with the IEEE 1149.1 test bus. PWB test advantages using the IEEE 1149.1 test bus are much more obvious since PWB test problems are more challenging.

Partitioning

Partitioning is always a very important design consideration for PWB test. Any medium-to-high complexity PWB must have adequate partitioning to allow independent testing of major logic functions. In most designs, testable partitions can be created by simply replacing the normal buffers and transceivers, which are already required in the design, with SCOPE bus-interface products. The SCOPE bus-interface products perform the same buffer, latch, or transceiver function, but now they can be controlled via the IEEE 1149.1 test bus to load or sample signal states during design verification, test, and debug.

For instance, consider the simple microprocessor board design shown in Figure 5. In order to execute test software, the processor, memory, glue-logic ASIC, IC, and PWB interconnects must be fault free. If a fault exists on the memory data bus, the processor will execute bad code and control will be lost. By adding boundary scan in the ASICs and replacing the bus transceivers with SCOPE bus-interface products, as shown in Figure 6, the processor, memory, and ASICs can be tested independently. This reduces the ambiguity group and results in better fault isolation. Repair and replacement savings can be realized by faster troubleshooting and fault isolation to fewer components. By using the partitioning provided by the SCOPE bus-interface products and ASICs with IEEE 1149.1, PWB failures can be detected and isolated with less probing or arbitrary part substitution.

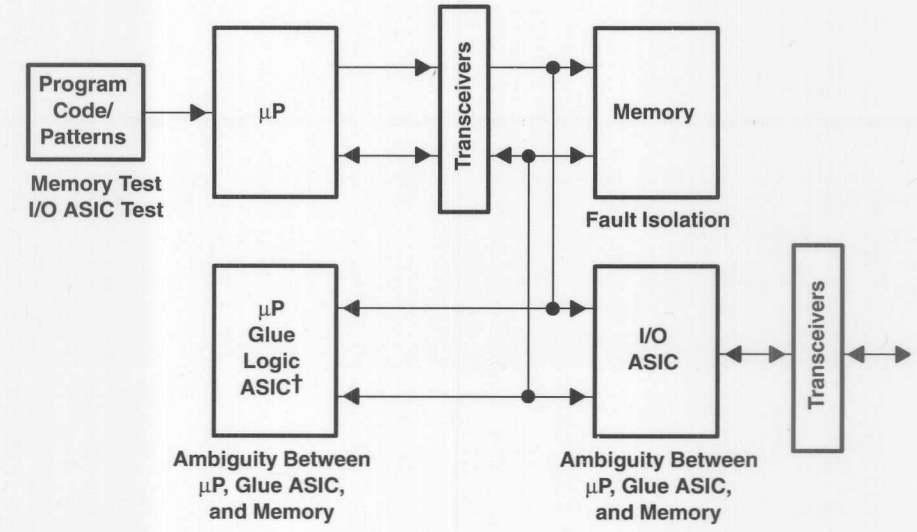
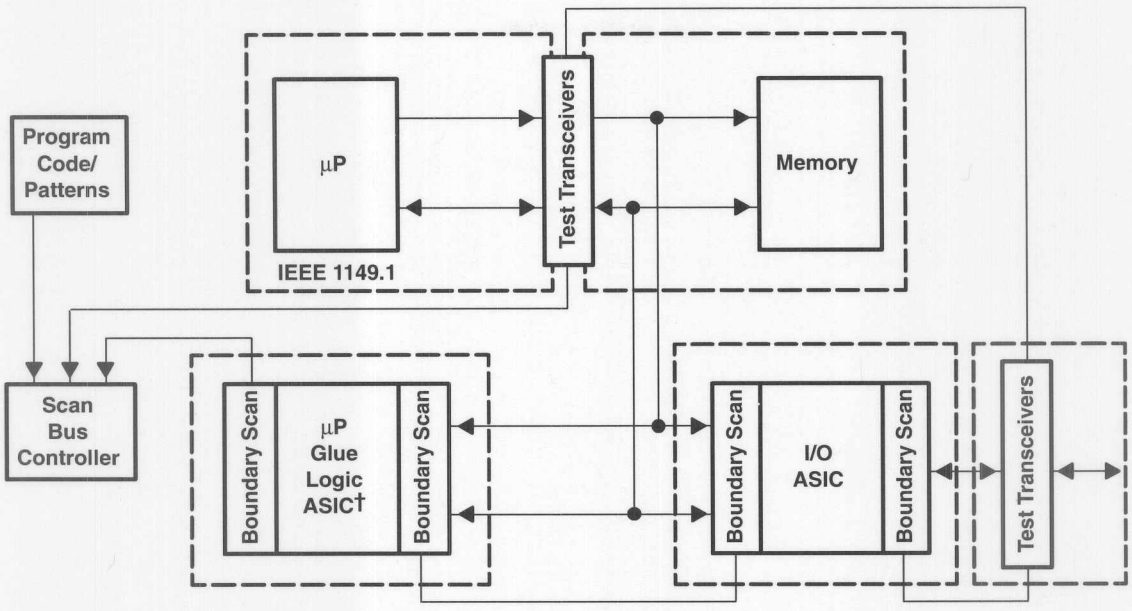


Figure 5. Simple Processor PWB Design



† Memory, decode, I/O decode, etc.

Figure 6. Design Partition Via Boundary Scan

Real Estate

The PWB test-logic real-estate impact can be minimized and, in some cases, PWB real estate can be gained by using IEEE 1149.1 to test functions. PWB real-estate savings can be accomplished by replacing an IC added for test purposes with boundary scan embedded in the IC silicon. Test logic that is added to meet fault detection or fault isolation can be efficiently implemented and controlled via the IEEE 1149.1 test bus.

In a recent design, several latches were added to capture and buffer some key internal bus-control signals for PWB test. If the internal bus is buffered by ASICs with boundary-scan or SCOPE bus-interface products, the signal states can be observed via the boundary-scan cells. This eliminates the need to add components for test purposes.

Test Points/Connector Size

IEEE 1149.1 boundary scan can be used to reduce or eliminate the number of test points or test pins on a PWB. When the four-wire IEEE 1149.1 test bus is brought out to the connector, many previously "hidden" internal nodes become visible. Boundary-scan cells can be thought of as virtual test points that can sample or control a node as shown in Figure 7. These virtual test points allow signal states to be scanned out and examined. Similarly, signal states can be scanned in and driven across circuit logic and interconnects. These control and observe operations can be performed via the IEEE 1149.1 test bus without the need to physically probe or route the signals under test to a test connector.

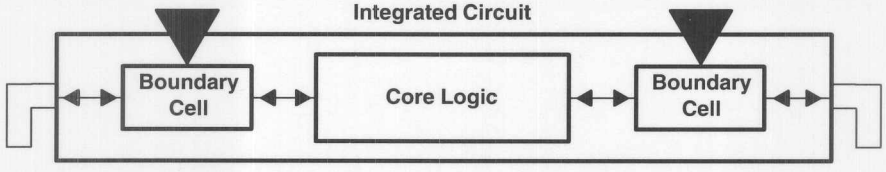


Figure 7. Virtual Test Points Via IEEE 1149.1 Boundary Scan

Two main advantages are obvious when using IEEE 1149.1 boundary scan as virtual test points. The first advantage is that fewer test points are required if critical signals are buffered by SCOPE bus-interface products or ASIC boundary cells. The second advantage is that boundary cells are not subject to the potential noise problems that may be caused by additional etch and pins of test points.

Reliability

PWB reliability usually will not increase significantly by adding IEEE 1149.1 to the design. The small increase in silicon gates may not be notable when compared at the PWB level. In fact, reliability may increase when ad hoc testability is replaced by IEEE 1149.1. Also, remember that the only impact to device functional logic reliability is the addition of the 2-to-1 multiplexer in the data path.

Another key factor to consider along with reliability is system availability. A small decrease in system reliability may not be important if system availability increases. Consider a system with a 200-hour MTBF and a repair time of ten hours. The system will have an availability of 1-10/200 = 95 percent. Now consider a more testable system that has a 195-hour MTBF and a repair time of only five hours. The system will have an availability of 1-5/195 = 97.5 percent.

Test Costs

PWB test costs can vary greatly with the complexity and testability of the design. Even simple designs without adequate testability can cause production slowdowns and cost overruns. Production test costs can account for a significant portion of the final product costs. In some businesses, it is estimated that 25% of the product costs result from test costs. Consider the following PWB-production test scenarios. A PWB has an ambiguity group of three high-cost parts using conventional functional-based test techniques. If the failure can be isolated to one device with boundary scan, savings can be realized because several good parts were saved as well as the labor and time required for unnecessary replacement. In another scenario, an hour of technician's labor, including overhead, is $20/hour, and a PWB test requires 10 minutes per PWB, producing 5,000 PWBs/month. If the added testability of IEEE 1149.1 provides a 20% reduction in PWB test times, the production test savings equal $3340 ($20 × 0.167 × 5,000 × 0.2) per month.

System Test

IEEE 1149.1 can also be used for system-level tests. The increased access afforded by the test and boundary scan allow control and observability in a closed system. Tests that previously required physical access using probe clips or extender boards can be performed via the IEEE 1149.1 bus. This reduces faults caused by the additional loading of test probes, electromagnetic interference, and manually-inducted removal and replacement.

PWB-to-PWB Interfaces

Extending the IEEE 1149.1 bus between PWBs can be accomplished by two basic methods: ring and star. The ring configuration allows a simple method to extend the PWB-level scan ring. However, this method has several drawbacks; the scan bus may become very long, which can slow test throughput, and a single-point failure caused by a broken connection or missing PWB will break the scan ring. The ring configuration from PWB-to-PWB interfacing is most practical for a small number of PWBs, typically four or less.

An IEEE 1149.1 star configuration between PWBs allows each PWB scan ring to be addressed without the overhead of additional PWBs in the scan path. However, this method requires additional backplane signals and allows only one PWB at a time to be addressed. Multiple PWBs cannot be scanned simultaneously with a star configuration.

There are several methods to efficiently partition scan rings from PWB to PWB. The simplest solution is to use the 'ACT8997 scan-path linkers or 'ACT8999 scan-path selectors to partition PWB scan rings. These devices allow a complete PWB scan ring to act as one device in bypass mode. This shortens a PWB scan ring to just one bit in the scan path. For more information on using scan-path selectors, see the article *Partitioning Designs With 1149.1 Scan Capabilities*.

Test-Bus Controllers (TBC)

Control of the IEEE 1149.1 test bus for system test can be accomplished via either an external TBC or via an internal embedded TBC. Figure 8 shows an example system with internal and external TBCs. For factory- or maintenance-type testing, a single external TBC will suffice as the IEEE 1149.1 master. Naturally, in this configuration, scan-based test can be performed only under external control.

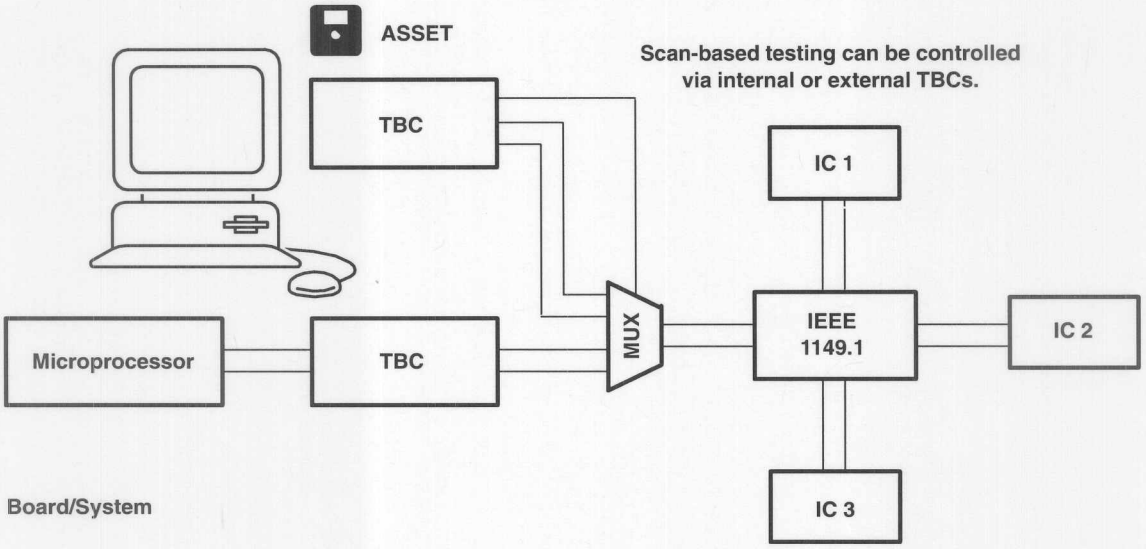


Figure 8. IEEE 1149.1 TBCs

The other option, an embedded TBC, allows autonomous testing under control of the embedded TBC. For small systems (less than four boards), a single TBC may be sufficient to test the system quickly. For larger or more complex systems, multiple TBCs may be required to test the system within an allocated time limit. The actual implementation method depends on the requirements for test execution time, real-estate limits, and fault tolerance.

Conclusion

Considering all the advantages that a standard test-bus and boundary-scan architecture provides, IEEE 1149.1 should be seriously considered as a test solution. While the capabilities gained are not free, the tradeoffs should be investigated. Advantages include increased controllability and observability, test reuse, better fault detection and isolation, and consistent test methods across multiple test environments. Impacts include cost, propagation delay of one 2-to-1 multiplexer in the signal path, and increased gate count for test logic. Although IEEE 1149.1 is suitable for all logic design sizes, implementing IEEE 1149.1 typically is easier to justify on larger designs. In the tradeoff analysis consider hidden costs such as fault-isolation size, test-development time, test-execution time, repair time, and life-cycle repair and maintenance cost. These costs should not be underestimated. Using the capabilities of the IEEE 1149.1, test bus and boundary scan provide advantages that help reduce the total cost of ownership.

Acknowledgment

The original author of this paper is Wayne Daniel.